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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/872,684	06/01/2001	Shelley Cheng	NSC1-D3620	3861

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EXAMINER

THOMPSON, MARC D

ART UNIT	PAPER NUMBER
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2144

DATE MAILED: 06/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/872,684

Applicant(s)

CHENG, SHELLEY

Examiner

Marc D. Thompson

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 19 April 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 14-21 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 14-21 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 12 July 2002 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

1. Amendment B, Paper #9, received 4/19/2004, has been entered into record.
2. Claims 14-21 remain pending.

Priority

3. This application is a divisional of parent patent application 09/048,468, now United States Patent Number 6,496,869, issued 12/17/2002.
4. The effective filing date for the subject matter defined in the pending claims in this application is 3/26/1998.

Drawings

5. The Examiner contends that the drawings submitted on 7/12/2002 are acceptable for examination proceedings.

Information Disclosure Statement

6. Examiner contends overlooking the first reference of the patented documents recited on the IDS, Paper #2, filed on 6/1/2001. While this reference was indeed reviewed, consideration was not clear on the record. A revised, fully initialed IDS is enclosed herewith in regard to the patented documents submitted for review by the Office.
7. The NPL references previously not considered due to their absence have been retrieved from the parent patented file. Copies are now available in the present application as indicated on the enclosed PTO-892.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

9. Claims 14-21 are rejected under 35 U.S.C. §103(a) as being unpatentable over Hill et al. (U.S. Patent Number 5,796,944), hereinafter referred to as Hill, in view of Davie, "A Host-Network Interface Architecture for ATM", ACM SIGCOMM, Volume 21, Issue 4, pp.307-315, August 1991, hereinafter referred to as Davie.

10. Hill disclosed a network interface card operating to process, store, forward, filter, segment, reassemble, receive and transmit network frames. See, inter alia, Column 4, Lines 3-24, and Column 5, Lines 44-62. The teachings further described express buffer management. See, inter alia, Column 2, Lines 35-54, and Column 4, Lines 17-20. Thus, the reception of network frames, subsequent buffering of these frames controlled by a buffer manager, and one type of filtering of incoming framed data was disclosed. See, inter alia, Column 4, Lines 57-64, and Column 7, Lines 28-45. In short, the MAC acted to filter frames accepted into the buffer memory system(s) based on destination and terminal addressing mechanisms. Subsequent to frame acceptance, further frame processing and filtering was also disclosed, inter alia, in Column 13, Lines 39-56. Hill expressly disclosed buffer management functionality through use of the Buffer Management ASIC (BMA)(22), using multiple word addressing and storage, sequential addresses in buffer memory(ies), and specific address management using an Address Management ASIC(32). See, inter alia, Column 2, Lines 35-54, Column 4, Lines 3-24, Column 7, Lines 13-27, and Column 14, Lines 12-33.

11. Lastly, Examiner notes the totality of the Hill disclosure as encompassing several hundred more pages of technical description (inter alia, Column 5, Lines 15-20, Column 6,

Lines 5-13, and Column 7, Lines 40-45) which are not currently referenced or currently cited, but should not be entirely ignored. These documents are fully incorporated by reference into the Hill document, itself being provided by Applicant, and may contain features of the claimed invention not yet present.

12. While Hill disclosed the invention substantially as claimed, Hill did not expressly disclose the writing of a second frame into receive buffer memory while another, first (previously transferred) frame is simultaneously being read out of the reception buffer memory. Since Hill dealt directly with high speed network packet processing and transfer with a variety of media (i.e., network) types (Column 1, Lines 12-45), and the movement of network information to the memory of an arbitrary host machine, an ordinary artisan would have been motivated to search the related arts for teachings related to the access of information from a host looking to access received information. In the same art of high speed network interfacing, Davie disclosed the use of dual-ported memory in conjunction with direct memory access (DMA) transfer of information to a host processor.

13. In short, Davie disclosed the combination of the transfer (reading) of buffer memory by/to a host memory segment, while the network interface continued to receive information from the network, also being buffered under the control of buffer management. See, inter alia, Pages 310-311, and Figures 2 and 3. The use of dual-port memory allowed simultaneous access to previously buffered frame data received from the network and currently frame data being buffered. See, inter alia, Sections 3.1 and 4.1.

14. It would have been obvious to one of ordinary skill in the art at the time of invention to modify the internetworking frame processing system of Hill with the frame processing using

dual-port memory provided by Davie in order to increase the speed of transfer of received frame information into host memory for suitable network or transport layer protocol processing, perhaps specifically destined for that particular network device.

15. Since the claimed invention recite elements found within this combination of teachings, claims 14-21 are rejected.

16. Claims 14-21 are rejected under 35 U.S.C. §103(a) as being unpatentable over Petersen et al. (U.S. Patent Number 5,299,313), hereinafter referred to as Petersen, in view of Gaddis et al. (U.S. Patent Number 5,815,501), hereinafter referred to as Gaddis.

17. Petersen disclosed buffer management and frame reception and filtering, where the memory containing the buffers for frame reception and transmission staging was distinct from host based memory. See, inter alia, Column 1, Line 60 through Column 2, Line 14. The received frame data was transferred to the host memory using specific logic for this purpose (i.e. upload DMA logic). See, inter alia, Column 2, Lines 48-51, and Column 8, Line 64 through Column 9, Line 21. Typical media access control to buffer functionality was expressly disclosed, inter alia, in the background of the invention at Column 1, Lines 23-31, including well known filtering of frame data segments intended for particular terminals. Petersen disclosed interfacing the host bus (EISA) and controlling the use of this bus for information transfer to the host memory and processor. See, inter alia, Column 6, Lines 4-28.

18. Since the RAM interface bus (50) was disclosed as distinctly different from the host bus interface (51) (e.g., EISA) (Figure 2, and Column 5, Lines 4-13), an artisan of ordinary skill in the art at the time of invention would have been motivated to explore bus contention teachings to

minimize any inherent delay during the use of these buses; that is, the disclosed designation of master/slave status of the host bus, the provision for Master/Slave “union”, and associated discussion of buss usage would have motivated an ordinary artisan at the time of invention to explore related bus arbitration arts to maximize functionality of the invention as a whole. Additionally, an ordinary artisan implementing the Petersen teachings would have been motivated to search the related arts for similar network processing methodologies in order to take advantage of any isolated improved functionality.

19. In the same art of high speed network frame processing, Gaddis disclosed the use of dual port memory modules in a network processing device which functioned to isolate the two buses (i.e., the host bus, and the network adapter/network bus). See, inter alia, Column 1, Line 52 through Column 2, Line 35, and Column 6, Lines 56-67. This directly dealt with bus contention, simultaneous access of shared memory segments, as well as disclosing many similar details well known in a network processing environment – buffer management, DMA transfer of host destined information, filtering host framed information, FIFO usage, and various media types (i.e., Ethernet and ATM interfacing). The teachings of Gaddis provided further, enhanced functionality of a typical network processing device known in the art at the time of invention.

20. It would have been obvious to modify the system of Petersen with the teachings of Gaddis in order to, minimally, enhance DMA transfer of information to a host memory segment, as well as eliminating bus contention by physically isolating the buses from each other without significant modification to the overall structure of Petersen.

21. Thus, since the combination of Petersen and Gaddis disclose all the claimed limitations as set forth in the claimed invention, claims 14-21 are rejected.

Response to Arguments

22. The arguments presented by Applicant in the response, Amendment B, Paper #9, received 4/19/2004, are not considered persuasive.

23. Applicant argues the prior art as applied fails to teach “media access control (MAC) configured to filter incoming frame data to determine whether to accept such data” and subsequent “[reception] of the frame data by the buffer manager”. See, inter alia, Response, Amendment B, Paper #9, received 4/19/2004, Page 6, Lines 11-19. As it was attempted to make clear in the previous Office action (See, Paper 6, Page 10, Paragraph 29, first 5 lines), the rudimentary filtering of frame data at the logical MAC layer was well known at the time of invention. Applicant further contends “the element of Hill’s system which performs filtering of data received from a network is frame processor unit (FPU) 40”. See, inter alia, Response, Amendment B, Paper #9, received 4/19/2004, Page 6, Lines 20-22. Page 7 reiterates the same argument again and again. It is respectfully submitted that Applicant has misconstrued the interpretation provided by the Examiner and fails to recognize the breadth of the claims currently presented. There are at least two (2) filtering operations occurring in Hill’s system. First, the frames are filtered from the network at the MAC layer *in order to determine whether the frame is intended to be processed by the receiving terminal*. The function of MAC was exactly this, to manage access to the physical network and delimit frames in the lower two logical layers (physical and data-link) of the ISO OSI networking model for subsequent delivery of information to the appropriate end station (networking address layer of model). On all Ethernet MAC controllers (inter alia, Hill, Column 4, Lines 3-6) traffic on the Ethernet network coupled to the MAC controller was seen by all terminals on the Ethernet network. Each terminal was

responsible for “filtering” the data to be “forwarded” up a particular protocol stack for subsequent processing based on whether the frames were actually destined for this (or a subsequent) particular terminal. Memory, especially finite and limited buffer memory, was not generally used to store information which would not be processed. Thus, the MAC controllers (16) as taught by Hill receive and filter the Ethernet frames which are subsequently processed and stored by the buffer manager (22). Further filtering was also evident using FPU (40), but this does not preclude the initial filtering of Ethernet (and other) frames arriving from the network(s), effecting storage, resultant buffering, and potential processing of these frames, including further filtering. Thus, the provision for frame filtering at the logical MAC layer is not considered to be a patentable distinction, since this functionality was inherent in line interface circuitry connecting a network interface card to a physical network, notoriously widely implemented in the art at time of invention.

24. In the Response, Amendment B, Paper #9, received 4/19/2004, Pages 8 and 9 follow the same type of argument lines, where a delineation between MAC layer filtering and actual frame filtering seems to be the point of contention. Following the same reasoning as set forth above, since the amended subject matter as broadly claimed was a required, normal operating procedure of typical network interface(s), no weight can be given to any distinction between the features as argued and the prior art of record as applied. It is noted that it is possible that Applicant is assigning some different meaning to the term “filtering” (which could force interpretation of processing at a higher level, for example, detecting command messages), but put simply, these functional features are simply not claimed. Although the claims are interpreted in light of the

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specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

25. Examiner maintains previously asserted Official Notice (see MPEP §2144.03) of well known subject matter. The connection of media access control (hardware/software) to a media interface (network bus), configured to filter incoming frame data (determine if frame was to be processed for further processing on this terminal) is fully maintained. Applicant is invited to argue any potential differences as alleged between the claim amendments and this basic networking interfacing fact in order to determine any differences between them. Further (as previously asserted) the use of a "buffer manager" (memory storage manager) coupled with the MAC (network media) configured to receive frame data, use of circular and first-in, first-out (FIFO) incoming and outgoing buffers, and a memory wherein the buffer manager wrote the frame data (for storage), and lastly, "dual port memory" for simultaneous access (i.e., reading and writing) from two distinct information transport buses (namely, the host processing bus and the network interface card bus), were all notoriously well known in the art at the time the invention was made. None of these features, alone or in combination will be considered to hold any substantial patentable weight. It is also noted that direct memory access (DMA) techniques were widely utilized in related arts for many, many years prior to the filing of the instant invention. DMA operations typically allowed direct usage of host based memory segments for storage of received network frames. Since these transactions occur on the system bus, there is no contention on the network card bus, allowing simultaneous transfer of information from the network to the card, and the card to the host, as claimed. All these functional elements were well

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known in the art, and are easily verifiable in the prior art previously submitted and currently cited.

Thus, the Examiner remains firm that the invention as set forth in claim 1 (and a number of the dependent claims), were notoriously well known in the art at the time the invention was made, as seen by the disclosure of prior art in the present specification, submitted prior art documentation, newly cited prior art, and the above non-challenged Official Notice functionality. The described functionality and claimed components were commonly found on common network interface cards (with dual port RAM) available on the market well before and at the time the invention was made.

The Examiner wishes to maintain that the Applicant is entitled to traverse any/all official notice taken in this action according to MPEP § 2144.03, even though a seasonable challenge has not been timely made. A “seasonable challenge” is an explicit demand for evidence set forth by Applicant in the next response. Accordingly, while the claim limitations the Examiner considered as “well known” in the first Office action may now established as admitted prior art of record for the course of the prosecution (*In re Chevenard*, 139 F.2d 71, 60 USPQ 239 CCPA 1943), an opportunity to clarify the point of novelty of the invention remains available.

26. Lastly, as a general matter, not only the specific teachings of a reference but also reasonable inferences which an artisan would have logically drawn therefrom may be properly evaluated in formulating a rejection. *In re Preda*, 401 F.2d 825, 159 USPQ 342 (CCPA 1968) and *In re Sherpard*, 319 F.2d 194, 138 USPQ 148 (CCPA 1963). Skill in the art is presumed. *In re Sovish*, 769 F.2d 738, 226 USPQ 771 (Fed. Cir. 1985). Furthermore, artisans must be presumed to know something about the art apart from what the references disclose. *In re Jacoby*,

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309 F.2d 738, 226 USPQ 317 (CCPA 1962). The conclusion of obviousness may be made from common knowledge and common sense of a person of ordinary skill in the art without any specific hint or suggestion in a particular reference. *In re Bozek*, 416 F.2d 738, 1385 USPQ 545 (CCPA 1969). Every reference relies to some extent on knowledge of persons skilled in the to complement that which is disclosed therein. *In re Bode*, 550 F.2d 656, 193 USPQ 545 (CCPA 1977). Finally, *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971), clearly states “any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning, but so long as it takes into account only knowledge which was within level of ordinary skill at the time claimed invention was made and does not include knowledge gleaned only from applicant’s disclosure, reconstruction is proper”. Since the subject matter as set forth in the claims was well known at the time of invention, the Examiner contends that significant modification and clarification of the claims and claimed functionality occur before discussion of patentability begins. Amendments provided in the most previous response do not serve to clarify any point(s) of novelty. Applicant is once again encouraged to amend the claims, and discuss, in extreme detail, the functionality set forth in the claims, and how this functionality differs from what was known in the art and the art as currently applied.

Conclusion

27. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after

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the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

28. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Marc D. Thompson whose telephone number is 703-308-6750. The examiner can normally be reached on Monday-Friday, 9am-4pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William Cuchlinski, Jr. can be reached on 703-308-3873. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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